AMENDMENTS TO THE SPECIFICATION

Please replace the title of the invention with the following rewritten title:

SEMICONDUCTOR DEVICE FORMED ON AN SOI STRUCTURE WITH A STRESS-RELIEF LAYER

Please replace the paragraph beginning at page 2, line 22 with the following rewritten paragraph:

However, the ~~non-patent~~ above-described document [[1]] reports the result that the transconductance (gm) of the NMOSFET is more reduced in the SOI device than in the bulk device. This report is in the case of using LOCOS (Local Oxidation Of Silicon) for device isolation; the transconductance is greatly reduced as the oxide film is thicker. Inversely, in the PMOSFET, the transconductance is increased as the oxide film is thicker. This is because the oxide film (SiO2 film) in the device isolation region is expanded in volume to apply compressive stress to the SOI film. A reduction in the current value caused by the stress is nearly 40% at the maximum, and the merits of the SOI device are cancelled. Therefore, it is important to reduce the stress.

Please replace the paragraph beginning at page 9, line 3 with the following rewritten paragraph:

As described above, in the traditional structure, the stress is applied to the SOI film by the difference between thermal expansion coefficients of the BOX film and the SOI film. In the

embodiment, the stress-relief film 43 is disposed to suppress or prevent the downward warp as shown in Fig. 7. More specifically, the stress-relief film 43 has almost the same thermal expansion coefficient as that of the SOI film 25, and it is contracted by the same extent as the SOI film 25 with temperature drop from the temperature that silicon oxide becomes viscous. Therefore, when only the upper BOX film 44 and the stress-relief film 43 are disposed, the multilayer film is warped upward. In a three-layer structure as the embodiment in which the SOI film 25 and the stress-relief film 43 are disposed above and below the upper BOX film 44 so as to sandwich it, to be warped downward or upward is determined by the thermal expansion coefficient and thickness of the SOI film 25 on the upper side and the stress-relief film 43 on the lower side. As described above, in the embodiment, the thermal expansion coefficients of the SOI film 25 and the stress-relief film 43 are almost the same, and thus it is determined only by the thickness. This three-layer structure will be warped upward because the stress-relief film 43 on the lower side is thicker in the embodiment. Actually, it is not as easy as described above, because there are other layers including the lower BOX film 42 in addition to the three layers and there is the influence of the device isolation film 26. However, it is apparent that the SOI film and the thick BOX film disposed thereunder can suppress the tendency to be warped downward more than the traditional structure can. Consequently, the tendency of the SOI film 25 to be warped downward is suppressed in this manner. Therefore, reductions in the SOI MOSFET characteristics caused by the stress can be suppressed.

Please replace the paragraph beginning at page 10, line 14 with the following rewritten paragraph:

As described above, since the stress applied to the SOI film 25 is reduced as the stress-relief film 43 is thicker, it is fine that the stress-relief film 43 is as thick as possible from this point. On the other hand, when it is too ~~much thicker~~thick, etching becomes difficult in the later process (in forming the device isolation film by STI). Then, the film thickness of the stress-relief film 43 is formed nearly equal to the film thickness of the lower BOX film.

Please replace the paragraph beginning at page 10, line22 with the following rewritten paragraph:

Moreover, the upper BOX film 44 is formed thinner to reduce the stress which is applied to the SOI film 25 and the stress-relief film 43 because the thermal expansion coefficient of the upper BOX film 44 is smaller than that of the SOI film 25 or stress-relief film 43. The reduced stress is shared by the SOI film 25 and the stress-relief film 43; the ratio is greater in the thicker stress-relief film 43. In the meantime, the lower BOX film 42 is relatively thick to generate a great stress because the thermal expansion coefficient is relatively small. However, most of the stress is applied to the stress-relief film 43, and hardly applied to the SOI film 25.

Please replace the paragraph beginning at page 15, line 20 with the following rewritten paragraph:

Furthermore, in the embodiment, the stress-relief film 43 is formed of polysilicon, but it may be formed of amorphous silicon or crystalline silicon. (There is no great differencedifferent between polysilicon and amorphous silicon. Amorphous silicon is turned to be polysilicon in the process of annealing.)